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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/905,195	07/16/2001	Nobuaki Shinmori	KAN 135	3051
23995	7590	06/03/2005	EXAMINER	
RABIN & Berdo, PC 1101 14TH STREET, NW SUITE 500 WASHINGTON, DC 20005			DUNCAN, MARC M	
			ART UNIT	PAPER NUMBER
			2113	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/905,195

Applicant(s)

SHINMORI, NOBUAKI

Examiner

Marc M. Duncan

Art Unit

2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 March 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,4 and 8 is/are rejected.
- 7) ☒ Claim(s) 2,3,5,6,9 and 10 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 August 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Status of the Claims***

Claims 1 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al. in view of Mayer.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata and Mayer as applied to claims 1 and 8 above, and further in view of Grimmer, Jr et al.

Claims 2-3, 5-6 and 9-10 are objected to.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al. in view of Mayer.

Regarding claim 1:

Iwata teaches a JTAG port in Fig. 1 –11.

Iwata teaches a flash ROM that stores a security bit in Fig. 1 – 5 and column 4 line 64-col. 5 line 6.

Iwata teaches a TAP that communicates with the flash ROM in Fig. 5 – 31, col. 5 lines 63-col. 6 line 3 and col. 8 lines 29-33.

Iwata teaches a JTAG control circuit connected between the JTAG port and the TAP in Fig. 5 – 15.

Iwata does not explicitly teach the JTAG control circuit controlled by the security bit of the flash ROM. Iwata does not explicitly teach the JTAG control circuit allowing or preventing communication of signals between the JTAG port and the TAP depending on the state of the security bit. Iwata does, however, teach the JTAG controlling communications between the JTAG port and the TAP and also teaches preventing communications based on the state of the security bit in col. 5 line 63-col. 6 line 2 and col. 18 line 47-col. 19 line 10.

Mayer teaches controlling communications between a JTAG interface and a TAP with an on-chip control circuit in col. 4 lines 1-13.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the JTAG control circuit of Iwata with the access authorization circuit of Mayer.

One of ordinary skill in the art at the time of invention would have been motivated to make the combination because Mayer discloses that the use of such a system allows the risk of misuse of the JTAG interface to be kept to a minimum and allows for greater security of internal registers and memories of a circuit. Furthermore, the on-chip circuit

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of Mayer does not require the debugger be able to read and compare the security codes and perform access blocking.

Regarding claim 8:

Iwata teaches a memory device to store a control program and data in col. 1 lines 60-64.

Iwata teaches a central processing unit to execute a specific process according to the program in col. 2 lines 41-46 and col. 6 lines 5-24.

Iwata teaches a test port to input and output test signals in col. 5 lines 63-66.

Iwata teaches controlling on/off between the test port and the central processing unit in col. 1 line 64-col. 2 line 5 and col. 4 line 64-col. 5 line 6.

Iwata teaches controlling the on/off if the security bit has been changed to a predetermined state and based on a match of input data with data stored in the memory device in col. 18 line 47-col. 19 line 10.

Iwata does not explicitly teach a switch controlling the on/off. Iwata does not explicitly teach security control means for selectively turning off the switch and for comparing data input via the test port with the data stored in the memory and turning on the switch when the data agree. Iwata does, however, teach controlling the on/off if the security bit has been changed to a predetermined state and based on a match of input data with data stored in the memory device in col. 18 line 47-col. 19 line 10.

Mayer teaches a switch controlling the on/off in col. 4 lines 43-48. The inhibit signal controls the access authorization circuit to act as a switch. In one state the circuit is on and the data access is allowed. In the opposite state, the data flow is cut off.

Mayer also teaches comparing data input via the test port with the data stored in the memory and turning on the switch when the data agree in col. 4 lines 32-42.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Iwata with the switch function of Mayer.

One of ordinary skill in the art at the time of invention would have been motivated to make the combination because Mayer discloses that the use of such a system allows the risk of misuse of the JTAG interface to be kept to a minimum and allows for greater security of internal registers and memories of a circuit.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata and Mayer as applied to claims 1 and 8 above, and further in view of Grimmer, Jr et al.

Regarding claim 4:

The teachings of Iwata and Mayer are outlined above.

Iwata and Mayer do not explicitly teach the second data including a security bit being stored in a non-volatile register. Iwata and Mayer do, however, teach the second data including a security bit being stored in a non-volatile memory.

Grimmer teaches storing a security bit in a non-volatile register in the Abstract lines 16-17.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the security bit storage of Iwata and Mayer with the non-volatile register of Grimmer.

One of ordinary skill in the art at the time of invention would have been motivated to make the combination because storing the second data including the security bit in a

non-volatile register allows the security data to be stored permanently without using additional memory space.

### ***Allowable Subject Matter***

Claims 2-3, 5-7 and 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Prior art was not found that explicitly teaches or fairly suggests an inhibit gate having first and second terminals as outlined in claims 2 and 3. Prior art was not found that explicitly teaches or fairly suggests a logic gate turning on the switch when the two data agree, independent of the state of the security bit, as outlined in claims 5 and 6. Prior art was not found that explicitly teaches or fairly suggests the security means comprising a gate having an output connected to the switch and one of a plurality of input terminals connected to the security bit as outlined in claims 9 and 10.

### ***Response to Arguments***

Applicant's arguments concerning claim 1 have been fully considered but they are not persuasive.

Applicant argues that the JTAG control circuit cannot be connected between the JTAG port and the TAP and therefore could not allow or prevent communication between the TAP and the JTAG port. As can be seen from the above citations, the TAP is embedded in the JTAG control circuit and therefore the JTAG control circuit is clearly

between the TAP and the JTAG port and can easily prevent communications between the JTAG port and the TAP. The rejection is maintained.

Applicant's arguments with respect to claim 8 have been considered but are moot in view of the new ground(s) of rejection.


**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc M. Duncan whose telephone number is 571-272-3646. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

md

  
ROBERT BEAUSOLIEL  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100